Amended Claims With Mark-ups to Show Changes Made

1. (Amended) A test circuit for a microcontroller unit, comprising:

an input circuit that consists of,

a first pin receiving a first signal[;], and

a second pin receiving a second signal; and

a test signal generating circuit that generates a test signal in response to a logical combination of the first signal and the second signal.

2. (Amended) The circuit of claim 1, wherein the test signal generating circuit comprises:

a logic circuit that logically processes the first signal and the second signal;

a counter that is enabled and disabled based on an output signal from the logic circuit, wherein the [test mode] counter uses the second signal as a counting signal when enabled; and

a decoder that outputs the test signal when a count value from the counter reaches a prescribed count value.

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3. (Amended) The circuit of claim 2, wherein the [test mode] counter is disabled and reset when the output signal from the logic circuit is a low level.

5. (Amended) The circuit of claim [1, further] 2, comprising:

a test mode related circuit operated by the first signal and the second signal; and

an internal circuit that enters a test mode in accordance with the test signal from the test signal generating circuit, wherein the counter counts a plurality of prescribed values of the second signal.

8. (Amended) A microcontroller unit having a test mode setup circuit, the test mode setup circuit comprising:

a clock pin that receives a clock signal;

a reset pin that receives a reset signal;

a test mode counter that is set and reset based on the clock signal and the reset signal, wherein the [set] test mode counter counts the reset signal; and

a decoder that receives a count value from the test mode counter and activates a test mode flag when the count value reaches a prescribed value.

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12. (Amended) The microcontroller unit of claim 8, [further comprising] wherein the test mode setup circuit comprises:

[a clock pin receiving a clock signal;

a reset pin receiving a reset signal] an input circuit that consists of first and second pins, wherein the first pin is the clock pin and the second pin is the reset pin; and

an OR gate ORing the clock signal and the reset signal.

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